

AppKit:

Using the LTC1298 12-bit Analog-to-Digital Converter

This AppKit shows how to use the Linear Technology LTC 1298 12-bit ADC chip with PIC microcontrollers and the Parallax BASIC Stamp[®] single-board computer.

Description

The LTC1298 is a 12-bit analog-to-digital converter (ADC). It is internally referenced to the 5-volt power supply, providing voltage measurements with 1.22-millivolt resolution. It has an internal sample-and-hold feature that prevents errors when it is used to measure rapidly changing signals.

The LTC1298 can be configured as a two-channel ADC or single-channel differential ADC. In two-channel mode, the selected channel's voltage is measured relative to ground and returned as a value between 0 and 4095. In differential mode, the voltage difference between the two inputs is measured and returned as a value between 0 and 4095.

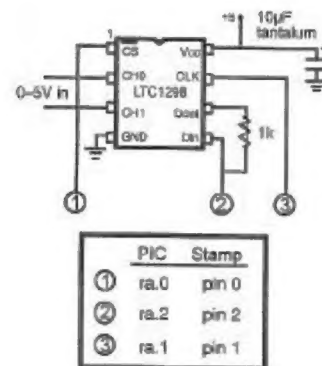
Supply current is typically 250 μ A when the unit is operating, 1 nA (one -billionth of an ampere) when it is not. The maximum clock rate for the LTC1298's three-wire serial interface is 200 kHz, permitting up to 11,100 samples to be taken per second.

Hardware interface

The LTC1298 interfaces with controllers through four pins: chip select (CS), clock (CLK), data in (DIN) and data out (DOUT). Since PICs can readily switch between input and output on the fly, the interface shown in the figure combines DIN and DOUT into a single connection.

As shown in the figure, the manufacturer recommends a 1- to 10- μ F bypass capacitor with good high-frequency qualities; a ceramic unit at the low end of the scale, tantalum at the higher end. Since the supply voltage also serves as the ADC's voltage reference, it must be well regulated to avoid measurement errors. Since the LTC1298 draws very little current, you may use a precision voltage reference Zener diode (such as the LM336) as a regulator.

See the manufacturer's documentation at the end of this App Kit for pcb design notes and analog characteristics.



PARALLAX

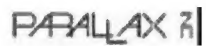
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 pictech@parallainc.com • stamptech@parallaxinc.com

Software Interface

From a software standpoint, using the LTC1293 boils down to this:

- (1) Activate CS by taking it low.
- (2) Send (shift out) configuration bits to the LTC1298.
- (3) Read (shift in) the 12-bit measurement from the LTC1298.
- (4) Deactivate CS by taking it high.

The program listings and data sheets show these processes in detail.



PIC Program Listing

```
; PROGRAM: LTC1298.SRC (Read LTC1298 analog-to-digital converter).
; Program demonstrates the use of an external serial ADC (Linear Tech
; LTC1298) with PIC16C5x-series controllers. Variable dc voltages
; (0-5V) at pins 2 or 3 of the ADC control the 12-bit value of the
; variable ADres.
```

```
CS          =          ra.0          ; Connect to CS pin of 1298.
CLK         =          ra.1          ; Connect to CLK pin.
DATA        =          ra.2          ; Connect to Din and Dout pins.
```

```
; Put variable storage above special-purpose registers.
```

```
org 8
Clocks      ds 1          ; Clock-cycle counter.
ADresH      ds 1          ; High byte of 12-bit ADC result.
ADresL      ds 1          ; Low byte of 12-bit ADC result.
Cnfig       ds 1          ; Holds configuration bits for ADC.

Startb      =          cnfig.0        ; Start-bit for conversation with ADC (always 1).
SglDif      =          cnfig.1        ; 1=single-ended, 2-ch; 0=differential, 1-ch
OddSign     =          cnfig.2        ; Selects ch 0 or 1 for input or + polarity.
MsbF        =          cnfig.3        ; MSBF mode select (always 1).
Xmit        =          0              ; TRIS setting to send data to LTC1298.
Recv        =          100b          ; TRIS setting to receive data from LTC1298.
FixBs       =          1001b         ; Fixed bits for configuration setting.
OutClk      =          4              ; Number of bits sent to LTC1298.
InClk       =          13             ; Number of bits received from LTC1298.
```

```
; Remember to change device info when programming part.
```

```
device      pic16c55,xt_osc,wdt_off,protect_off
reset       Start
```

```
; Set starting point in program ROM to zero
```

```
org 0
start      mov    lra, #xmit          ; Set TRIS ra to send configuration to ADC.
           mov    lrb, #0             ; Set TRIS rb and rc to output.
           mov    lrc, #0             ; Deselect LTC1298 for now.
           setb   CS
```

```
; Set up the configuration bits. A 1 in sglDif means a single-ended conversion;
; 0 means differential. For single-ended measurements, oddSign selects the channel:
; 0 = channel 0; 1 = channel 1. For differential conversions, oddSign selects polarity: 1
; = channel 1 +, 0 = channel 0 +.
```

```
setb       sglDif          ; Set for single-ended.
clrb       oddSign         ; Sample channel 0.
```



PIC Program Listing (cont.)

; Call the ADC subroutine.

```

        call      convert
        mov       rb, ADresL      ; Put the bits of ADC result on rb and rc.
        mov       rb, ADresH
        jmp       $              ; Stop program: results in registers 9 and A.

```

; This is the subroutine that gets the conversion from the LTC1298. Upon
 entry, the configuration bits must be set up in the cnfig register.
 ; Upon exit, the 12-bit result will be in ADresH/L. The cnfig register
 ; will have been restored to its original state.

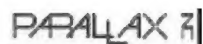
; This conversion routine will work properly at PIC clock speeds up to 8 MHz.
 ; Faster clocks will violate the LTC1298's max clock rate of 200 kHz. To slow
 ; the conversion routine, add more "jmp \$+1" 2-cycle delays in :loop1 and
 ; :loop2.

Convert

```

        mov       lrb,#xmit      ; Ready to transmit configuration to ADC.
        clrb      CLK           ; Begin with clock low.
        clrb      CS
        OR        cnfig,#fixBs   ; Write 1s to start and msbf bits
        mov       clocks,#outClk ; Set up number of config bits to write.
        clr       ADresL        ; Clear results registers.
        clr       ADresH
:loop1   rr        cnfig         ; Rotate bit 0 into carry.
        movb      DATA,c       ; Move carry bit to DATA pin.
        setb      CLK           ; Pulse the clock line.
        jmp       $+1
        clrb      CLK
        djnz      clocks,:loop1 ; Repeat for all config bits.
        rr        cnfig         ; Rearrange config register to original state.
        swap      cnfig
        mov       !rb,#recv      ; Change TRIS to input data.
        mov       clocks,#inClk  ; Set up number of data bits to receive.
:loop2   rl        ADresL        ; Rotate 16-bit ADres register left.
        rl        ADresH
        snb       DATA         ; Copy data bit to lsb of ADres.
        setb      ADresL.0
        sb        DATA
        clrb      ADresL.0
        setb      CLK           ; Pulse the clock line.
        jmp       $+1
        clrb      CLK
        djnz      clocks,:loop2 ; Repeat for all data bits.
        setb      CS           ; Deactivate the LTC1298.
        ret

```



BASIC Stamp I (BS1-IC) and BASIC Stamp Ver. D Program Listing

Program: LTC1298.BS1 (LTC1298 analog-to-digital converter)

The LTC1298 is a 12-bit, two-channel ADC. Its high resolution, low supply current, low cost, and built-in sample/hold feature make it a great companion for the Stamp in sensor and data-logging applications. With its 12-bit resolution, the LTC1298 can measure tiny changes in input voltage; 1.22 millivolts (5-volt reference/4096).

ADC Interface Pins

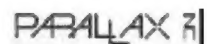
The 1298 uses a four-pin interface, consisting of chip-select, clock, data input, and data output. In this application, we tie the data lines together with a 1k resistor and connect the Stamp pin designated DIO to the data-in side of the resistor. The resistor limits the current flowing between DIO and the 1298's data out in case a programming error or other fault causes a "bus conflict." This happens when both pins are in output mode and in opposite states (1 vs 0). Without the resistor, such a conflict would cause large currents to flow between pins, possibly damaging the Stamp and/or ADC.

SYMBOL	CS = 0	Chip select; 0=active.
SYMBOL	CLK = 1	Clock to ADC; out on rising, in on falling edge.
SYMBOL	DIO_n = 2	Pin_number_of data input/output.
SYMBOL	DIO_p = pin2	Variable_name_of data input/output.
SYMBOL	ADbits = b1	Counter variable for serial bit reception.
SYMBOL	AD = w1	12-bit ADC conversion result.

ADC Setup Bits

The 1298 has two modes. As a single-ended ADC, it measures the voltage at one of its inputs with respect to ground. As a differential ADC, it measures the difference in voltage between the two inputs. The sglDif bit determines the mode; 1 = single-ended, 0 = differential. When the 1298 is single-ended, the oddSign bit selects the active input channel; 0 = channel 0 (pin 2), 1 = channel 1 (pin 3). When the 1298 is differential, the oddSign bit selects the polarity between the two inputs; 0 = channel 0 is +, 1 = channel 1 is +. The msbf bit determines whether clock cycles_after_the 12 data bits have been sent will send 0s (msbf = 1) or a least-significant-bit-first copy of the data (msbf = 0). This program doesn't continue clocking after the data has been obtained, so this bit doesn't matter.

You probably won't need to change the basic mode (single/differential) or the format of the post-data bits while the program is running, so these are assigned as constants. You probably will want to be able to change channels, so oddSign (the channel selector) is a bit variable.



BASIC Stamp I and Ver. D Program Listing (cont.)

SYMBOL	sglDif = 1	Single-ended, two-channel mode.
SYMBOL	msbf = 1	Output 0s after data transfer is complete.
SYMBOL	oddSign = bit0	Program writes channel # to this bit.

Demo Program

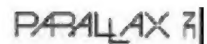
This program demonstrates the LTC1298 by alternately sampling the two input channels and presenting the results on the PC screen using Debug.

high CS	Deactivate the ADC to begin.
Again:	Main loop.
For oddSign = 0 to 1	Toggle between input channels.
gosub Convert	Get data from ADC.
debug "ch",#oddSign,";",#AD,cr	Show the data on PC screen.
pause 500	Wait a half second.
next	Change input channels.
goto Again	Endless loop.

ADC Subroutine

Here's where the conversion occurs. The Stamp first sends the setup bits to the 1298, then clocks in one null bit (a dummy bit that always reads 0) followed by the conversion data.

Convert:	
low CLK	Low clock-output on rising edge.
high DIO_n	Switch DIO to output high (start bit).
low CS	Activate the 1298.
pulsout CLK,5	Send start bit.
let DIO_p = sglDif	First setup bit.
pulsout CLK,5	Send bit.
let DIO_p = oddSign	Second setup bit.
pulsout CLK,5	Send bit.
let DIO_p = msbf	Final setup bit.
pulsout CLK,5	Send bit.
input DIO_n	Get ready for input from DIO.
let AD = 0	Clear old ADC result.
for ADbits = 1 to 13	Get null bit + 12 data bits.
let AD = AD%r*%r2+DIO_p	Shift AD left, add new data bit.
pulsout CLK,5	Clock next data bit in.
next	Get next data bit.
high CS	Turn off the ADC
return	Return to program.



BASIC Stamp II (BS2-IC) Program Listing

Program: LTC1298.BS2 (LTC 1298 analog-to-digital converter)

The LTC1298 is a 12-bit, two-channel ADC. Its high resolution, low supply current, low cost, and built-in sample/hold feature make it a great companion for the Stamp in sensor and data-logging applications. With its 12-bit resolution, the LTC1298 can measure tiny changes in input voltage; 1.22 millivolts (5-volt reference/4096).

ADC Interface Pins

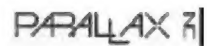
The 1298 uses a four-pin interface, consisting of chip-select, clock, data input, and data output. In this application, we tie the data lines together with a 1k resistor and connect the Stamp pin designated DIO to the data-in side of the resistor. The resistor limits the current flowing between DIO and the 1298's data out in case a programming error or other fault causes a "bus conflict." This happens when both pins are in output mode and in opposite states (1 vs 0). Without the resistor, such a conflict would cause large currents to flow between pins, possibly damaging the Stamp and/or ADC.

CS	con	0	Chip select; 0 = active
CLK	con	1	Clock to ADC; out on rising, in on falling edge.
DIO_n	con	2	Data I/O pin_number_.
config	var	nib	Configuration bits for ADC.
AD	var	word	Variable to hold 12-bit AD result.

ADC Setup Bits

The 1298 has two modes. As a single-ended ADC, it measures the voltage at one of its inputs with respect to ground. As a differential ADC, it measures the difference in voltage between the two inputs. The sgIDif bit determines the mode; 1 = single-ended, 0 = differential. When the 1298 is single-ended, the oddSign bit selects the active input channel; 0 = channel 0 (pin 2), 1 = channel 1 (pin 3). When the 1298 is differential, the oddSign bit selects the polarity between the two inputs; 0 = channel 0 is +, 1 = channel 1 is +. The msbf bit determines whether clock cycles_after_the 12 data bits have been sent will sent 0s (msbf = 1) or a least-significant-bit-first copy of the data (msbf = 0). This program doesn't continue clocking after the data has been obtained, so this bit doesn't matter.

You probably won't need to change the basic mode (single/differential) or the format of the post-data bits while the program is running, so these are assigned as constants. You probably will want to be able to change channels, so oddSign (the channel selector) is a bit variable.



BASIC Stamp II Program Listing (cont.)

startBvar	config.bit0	Start bit for comm with ADC.
sglDif var	config.bit1	Single-ended or differential mode.
oddSign	var	config.bit2 Channel selection.
msbf var	config.bit3	Output 0s after data xfer complete.

Demo Program

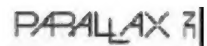
This program demonstrates the LTC1298 by alternately sampling the two input channels and presenting the results on the PC screen using Debug.

high CS	Deactivate ADC to begin.
high DIO_n	Set data pin for first start bit.
again:	Main loop.
for oddSign = 0 to 1	Toggle between input channels.
gosub convert	Get data from ADC.
debug "channel",DEC odd	Sign, ":",DEC AD,cr' Display data.
pause 500	Wait a half second.
next	Change channels.
goto again	Endless loop.

ADC Subroutine

Here's where the conversion occurs. The Stamp first sends the config bits to the 1298, then clocks in the conversion data. Note the use of the new BS2 instructions Shiftout and Shiftin. Their use is pretty straightforward here: Shiftout sends data bits to pin DIO and clock the CLK pin. Sending the least-significant bit first, it shifts out the four bits of the variable config. Then Shiftin changes DIO to input and clocks in the data bits--most-significant bit first, post clock (valid after clock pulse). It shifts in 12 bits to the variable AD.

convert:	
config = config 1 %1011	Set all bits except oddSign.
low CS	Activate the ADC.
shiftout DIO_n,CLK,lsbfirst,	[config\4] Send config bits.
shiftin DIO_n,CLK,msbpost	[AD\12] Get data bits.
high CS	Deactivate the ADC.
return	Return to program.





FEATURES

12-Bit Resolution

8-Pin SOIC Plastic Package

Low Cost

Low Supply Current: 250 μ A Typ.

Auto Shutdown to 1nA Typ.

Guaranteed $\pm 3/4$ LSB Max DNL

Single Supply 5V to 9V Operation

On-Chip Sample-and-Hold
60 μ s Conversion Time

Sampling Rates:

12.5 ksp/s (LTC1286)

11.1 ksp/s (LTC1298)

I/O Compatible with SPI, Microwire, etc.

Differential Inputs (LTC1286)

2-Channel MUX (LTC1298)

3V Versions Available: LTC1285/LTC1288

DESCRIPTION

The LTC1286/LTC1298 are micropower, 12-bit, successive approximation sampling A/D converters. They typically draw only 250 μ A of supply current when converting and automatically power down to a typical supply current of 1nA whenever they are not performing conversions. They are packaged in 8-pin SO packages and operate on 5V to 9V supplies. These 12-bit, switched-capacitor, successive approximation ADCs include sample-and-holds. The LTC1286 has a single differential analog input. The LTC1298 offers a software selectable 2-channel MUX.

On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

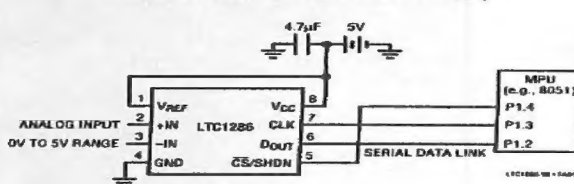
These circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (to 1.5V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

APPLICATIONS

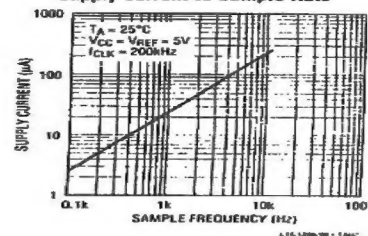
Battery-Operated Systems
Remote Data Acquisition
Battery Monitoring
Handheld Terminal Interface
Temperature Measurement
Isolated Data Acquisition

TYPICAL APPLICATIONS

25 μ W, SO-8 Package, 12-Bit ADC
Samples at 200kHz and Runs Off a 5V Supply



Supply Current vs Sample Rate



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND	12V	Power Dissipation	500mW
Voltage		Operating Temperature Range	
Analog and Reference	-0.3V to $V_{CC} + 0.3V$	LTC1286C/LTC1298C	0°C to 70°C
Digital Inputs	-0.3V to 12V	LTC1286I/LTC1298I	-40°C to 85°C
Digital Output	-0.3V to $V_{CC} + 0.3V$	Storage Temperature Range	-65°C to 150°C
		Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW VREF [1] 8 V_{CC} +IN [2] 7 CLK -IN [3] 6 DOUT GND [4] 5 CS/SHDN N8 PACKAGE 8-LEAD PLASTIC DIP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$	ORDER PART NUMBER LTC1286CN8 LTC1286IN8	TOP VIEW VREF [1] 8 V_{CC} +IN [2] 7 CLK -IN [3] 6 DOUT GND [4] 5 CS/SHDN S8 PACKAGE 8-LEAD PLASTIC SOIC $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 175^{\circ}\text{C/W}$	ORDER PART NUMBER LTC1286CS8 LTC1286IS8
			PART MARKING
			1286C 1286I
TOP VIEW CS/SHDN [1] 8 V_{CC} (V_{REF}) CH0 [2] 7 CLK CH1 [3] 6 DOUT GND [4] 5 DIN N8 PACKAGE 8-LEAD PLASTIC DIP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$	ORDER PART NUMBER LTC1298CN8 LTC1298IN8	TOP VIEW CS/SHDN [1] 8 V_{CC} (V_{REF}) CH0 [2] 7 CLK CH1 [3] 6 DOUT GND [4] 5 DIN S8 PACKAGE 8-LEAD PLASTIC SOIC $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 175^{\circ}\text{C/W}$	ORDER PART NUMBER LTC1298CS8 LTC1298IS8
			PART MARKING
			1298C 1298I

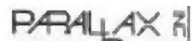
Consult factory for military grade parts.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (Note 3)	LTC1286	4.5		9.0	V
		LTC1298	4.5		5.5	V
t_{CLK}	Clock Frequency	$V_{CC} = 5V$	(Note 4)		200	kHz
t_{CYC}	Total Cycle Time	LTC1286, $t_{CLK} = 200\text{kHz}$	80			ns
		LTC1298, $t_{CLK} = 200\text{kHz}$	90			ns
??	Hold Time, D_{IN} After CLK	$V_{CC} = 5V$	150			ns
t_{aCS}	Setup Time CS Before First CLK (See Operating Sequence)	LTC1286, $V_{CC} = 5V$	2			ns
		LTC1298, $V_{CC} = 5V$	2			ns
t_{aDI}	Setup Time, D_{IN} Stable Before CLK	$V_{CC} = 5V$	400			ns
t_{WHCLK}	CLK High Time	$V_{CC} = 5V$	2			ns
t_{WLCLK}	CLK Low Time	$V_{CC} = 5V$	2			ns
t_{WHCS}	CS High Time Between Data Transfer Cycles	$V_{CC} = 5V$	2			ns
t_{WLCS}	CS Low Time During Data Transfer	LTC1286, $t_{CLK} = 200\text{kHz}$	75			ns
		LTC1298, $t_{CLK} = 200\text{kHz}$	85			ns



6-141



LTC1286/LTC1298

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1286			LTC1298			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution (No Missing Codes)		•	12			12			Bits
Integral Linearity Error	(Note 6)	•	±3/4	±2		±3/4	±2		LSB
Differential Linearity Error		•	±1/4	±3/4		±1/4	±3/4		LSB
Offset Error		•	¾	±3		¾	±3		LSB
Gain Error		•	±2	±8		±2	±8		LSB
Analog Input Range	(Note 7 and 8)	•	=0.05V to $V_{CC} + 0.05V$						V
REF Input Range (LTC1286)	$4.5 \leq V_{CC} \leq 5.5V$		1.5V to $V_{CC} + 0.05V$						V
(Notes 7, 8, and 9)	$5.5V \leq V_{CC} \leq 9V$		1.5V to 5.55V						V
Analog Input Leakage Current (Note 10)		•		±1			±1		AA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT'S
V_{IH}	High Level Input Voltage	$V_{CC} = 5.25V$	•	2			V
V_{IL}	Low Level Input Voltage	$V_{CC} = 4.75V$	•			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	•			2.5	AA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$	•			-2.5	AA
V_{OH}	High Level Output Voltage	$V_{CC} = 4.75V, I_O = 10I_A$	•	4.0	4.64		V
		$V_{CC} = 4.75V, I_O = 360I_A$	•	2.4	4.62		V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.75V, I_O = 1.6mA$	•			0.4	V
I_{OZ}	HI-Z Output Leakage	$CS = High$	•			±3	AA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			-25		MA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			45		MA
R_{REF}	Reference Input Resistance	$CS = V_{CC}$			5000		MY
	(LTC1286)	$CS = GND$			55		KY
I_{REF}	Reference Current (LTC1286)	$CS = V_{CC}$	•		0.001	2.5	AA
		$t_{CYC} \geq 640I_S, f_{CLK} \leq 25kHz$	•		90	140	AA
		$t_{CYC} = 80I_S, f_{CLK} = 200kHz$	•		90	140	AA
I_{CC}	Supply Current	$CS = V_{CC}$	•		0.001	±3.0	AA
		LTC1286, $t_{CYC} \geq 640I_S, f_{CLK} \leq 25kHz$	•		200	400	AA
		LTC1286, $t_{CYC} = 80I_S, f_{CLK} = 200kHz$	•		250	500	AA
		LTC1298, $t_{CYC} \geq 720I_S, f_{CLK} \leq 25kHz$	•		290	490	AA
		LTC1298, $t_{CYC} = 90I_S, f_{CLK} = 200kHz$	•		340	640	AA

DYNAMIC ACCURACY $f_{SAMPL} = 12.5kHz$ (LTC1286), $f_{SAMPL} = 11.1kHz$ (LTC1298) (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	1kHz/7kHz Input Signal		71/68		DB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	1kHz/7kHz Input Signal		-84/-80		DB
SFDR	Spurious-Free Dynamic Range	1kHz/7kHz Input Signal		90/86		DB
	Peak Harmonic or Spurious Noise	1kHz/7kHz Input Signal		-90/-86		DB

AC CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SAMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
$f_{SAMPL}(MAX)$	Maximum Sampling Frequency	LTC1286	•	12.5			KHz
		LTC1298	•	11.1			KHz
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{ADD}	Delay Time, CLK to DOUT Data Valid	See Test Circuits	•		250	600	Ns
t_{DS}	Delay Time, CS to DOUT Hi-Z	See Test Circuits	•		135	300	Ns
t_{EN}	Delay Time, CLK to DOUT Enable	See Test Circuits	•		75	200	Ns
t_{HDO}	Time Output Data Remains Valid After CLK	$C_{LOAD} = 100pF$			230		Ns
??	DOUT Fall Time	See Test Circuits	•		20	75	Ns
??	DOUT Rise Time	See Test Circuits	•		20	75	Ns
??	Input Capacitance	Analog Inputs, On Channel			20		PF
		Analog Inputs, Off Channel			5		PF
		Digital Input			5		PF

The • denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: These devices are specified at 5V. For 3V specified devices, see LTC1285 and LTC1288.

Note 4: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $t_{CLK} \geq 120kHz$ at 85°C, $f_{CLK} \geq 75kHz$ at 70° and $t_{CLK} \geq 1kHz$ at 25°C.

Note 5: $V_{CC} = 5V$, $V_{REF} = 5V$ and $CLK = 200kHz$ unless otherwise specified.

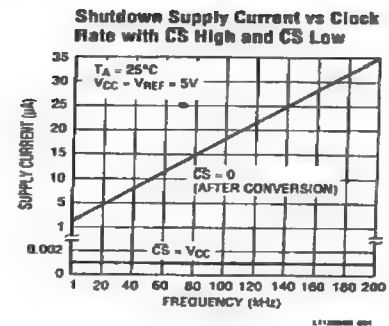
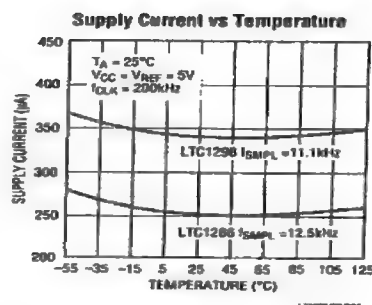
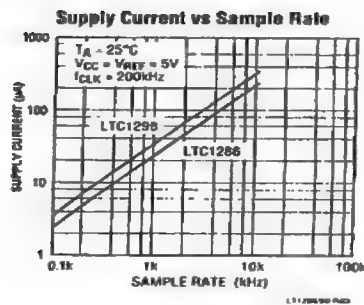
Note 6: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC} . This spec allows 50mV forward bias of either diode for $4.5V \leq V_{CC} \leq 5.5V$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading. For $5.5V < V_{CC} \leq 9V$, reference and analog input range cannot exceed 5.55V. If reference and analog input range are greater than 5.55V, the output code will not be guaranteed to be correct.

Note 8: The supply voltage range for the LTC1286 is from 4.5V to 9V, but the supply voltage range for the LTC1298 is only from 4.5V to 5.5V.

Note 9: Recommended operating conditions

Note 10: Channel leakage current is measured after the channel.

TYPICAL PERFORMANCE CHARACTERISTICS

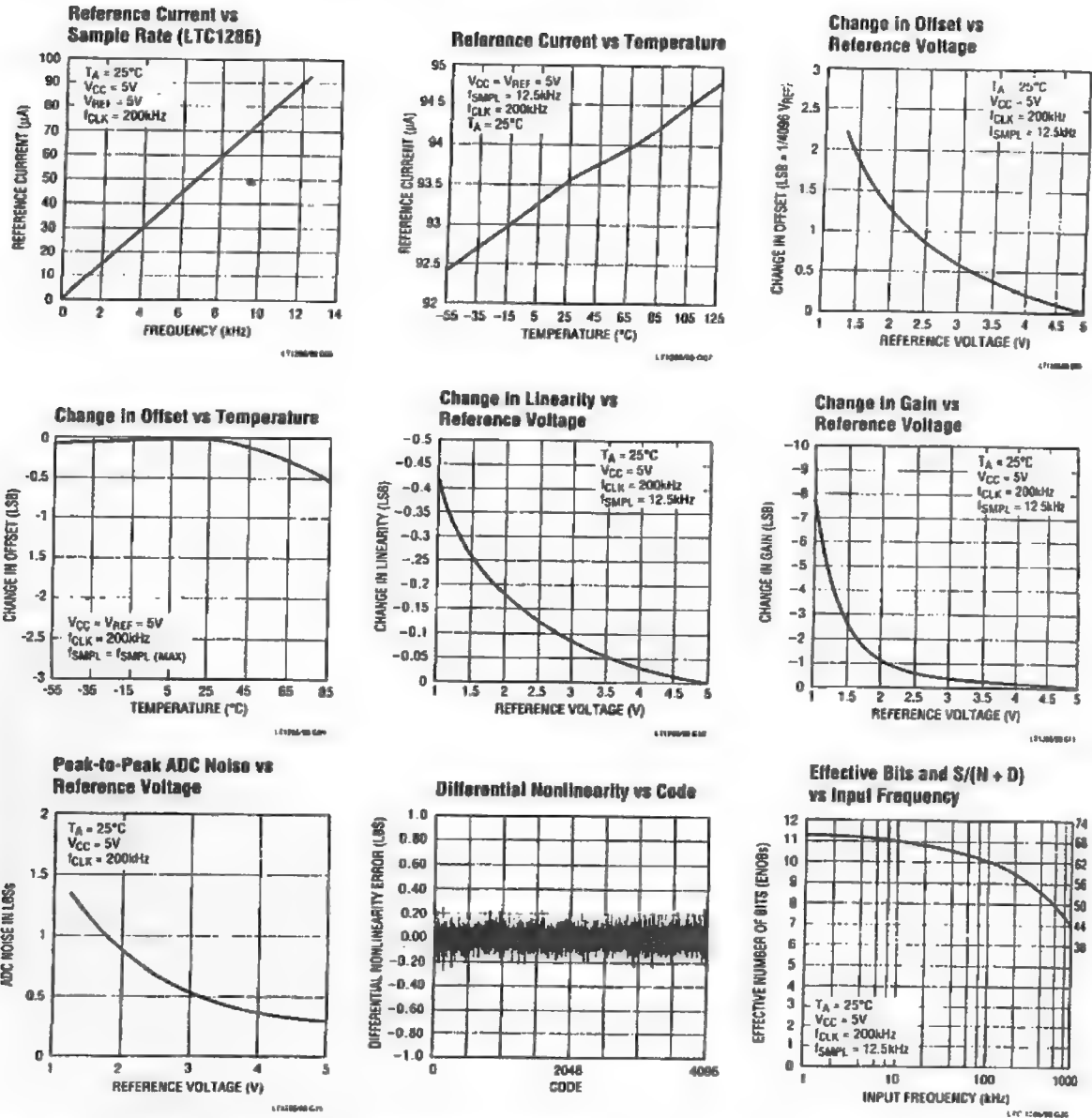
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PARALLAX

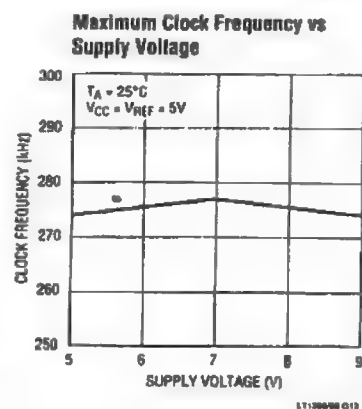
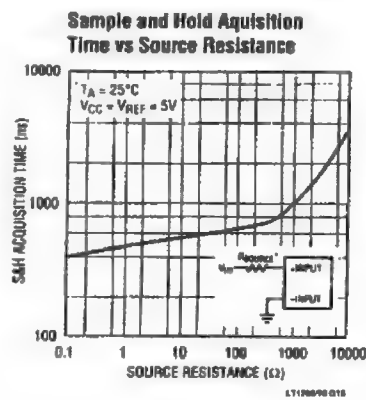
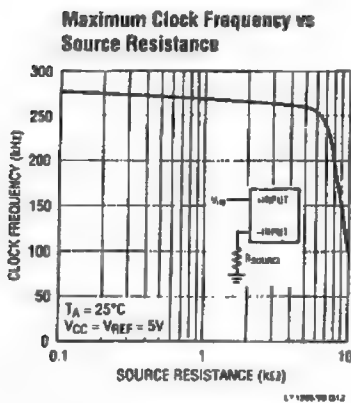
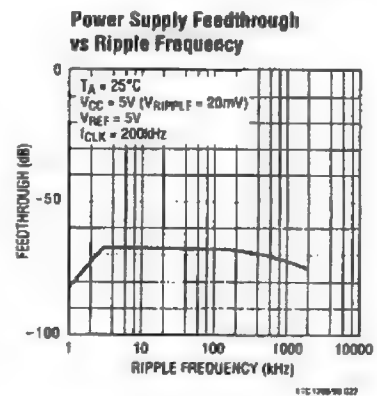
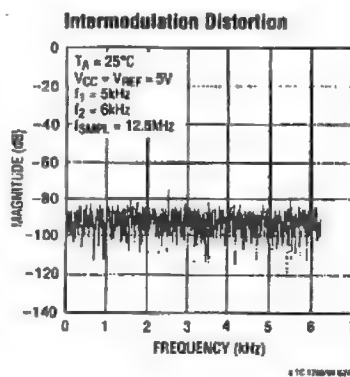
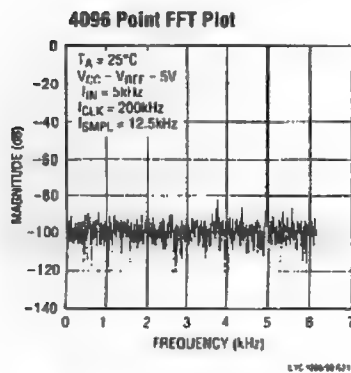
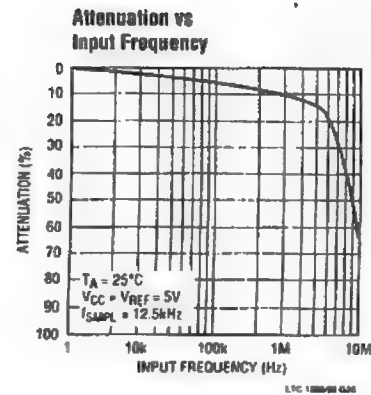
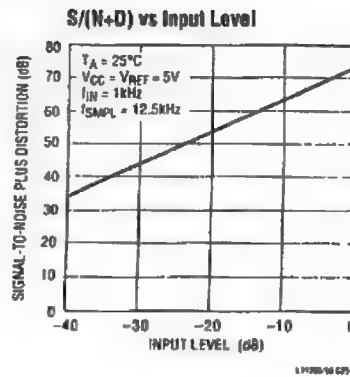
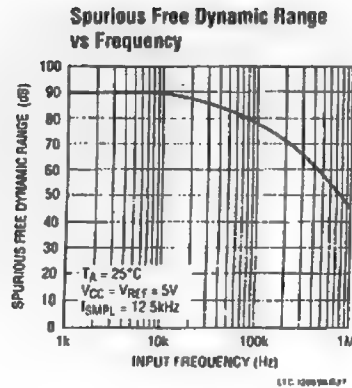
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LTC1286/LTC1298

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

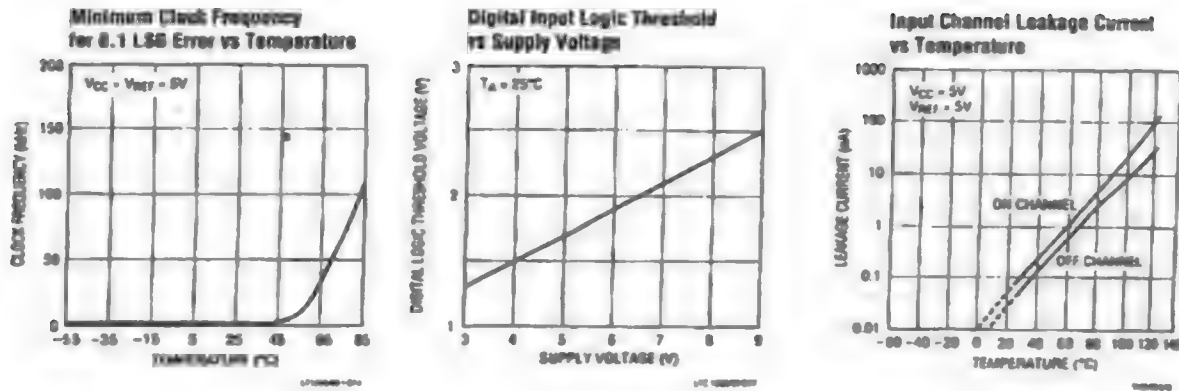


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LTC1286/LTC1298

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

LTC1286

VREF (Pin 1): Reference Input. The reference input defines the span of the A/D converter.

IN+ (Pin 2): Positive Analog Input.

IN- (Pin 3): Negative Analog Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CS/SHDN (Pin 5): Chip Select Input. A logic low on this input enables the LTC1286. A logic high on this input disables and powers down the LTC1286.

DOUT (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

VCC (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1298

CS/SHDN (Pin 1): Chip Select Input. A logic low on this input enables the LTC1298. A logic high on this input disables and powers down the LTC1298.

CHO (Pin 2): Analog Input.

CH1 (Pin 3): Analog Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

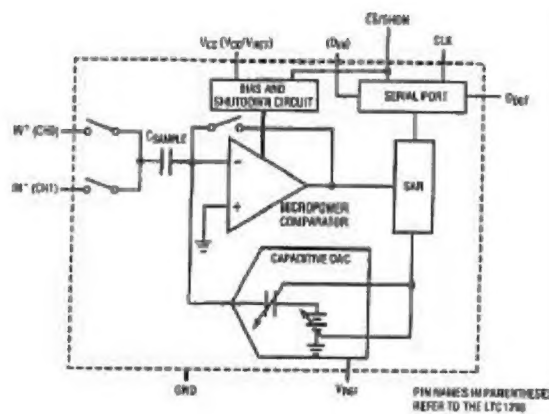
DIN (Pin 5): Digital Data Input. The multiplexer address is shifted into this input.

DOUT (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

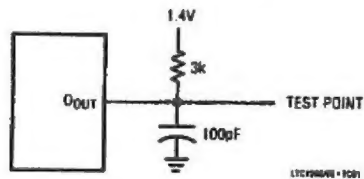
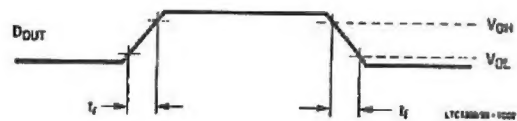
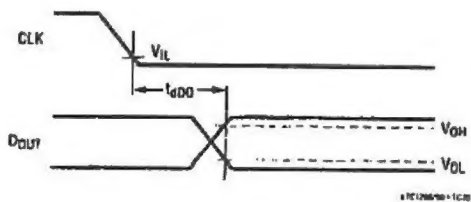
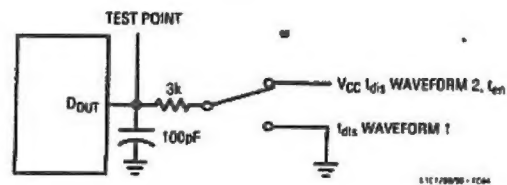
CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

VCC/VREF (Pin 8): Power Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

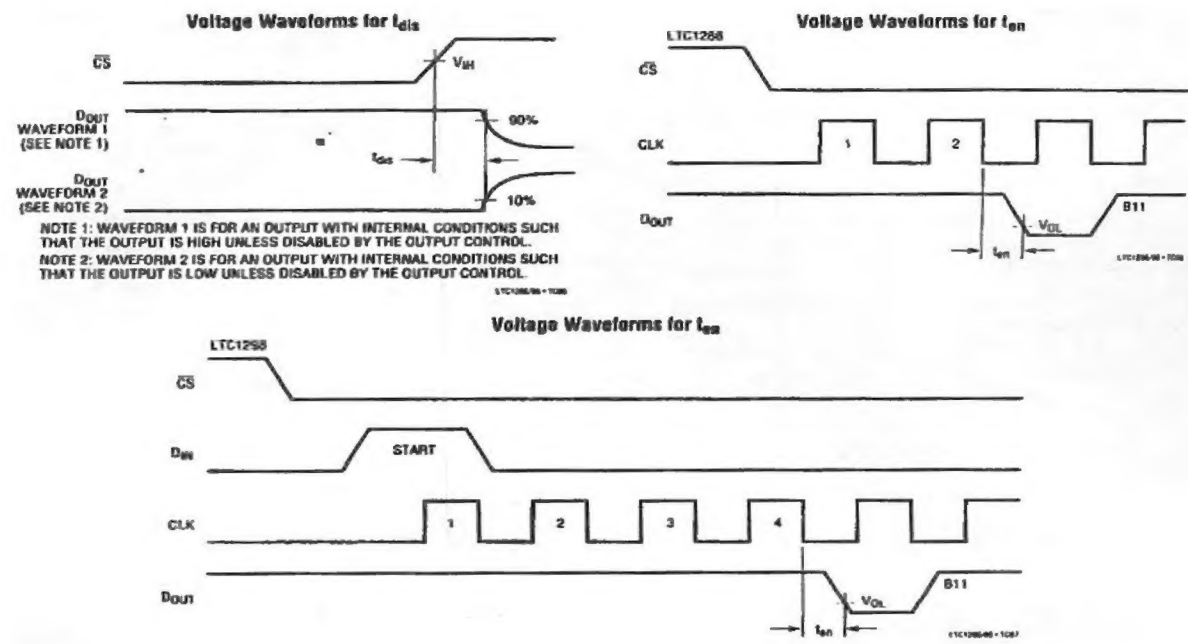


TEST CIRCUITS

Load Circuit for t_{d0} , t_r and t_f Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r , t_f Voltage Waveforms for D_{OUT} Delay Times, t_{d0} Load Circuit for t_{dis} and t_{en} 

LTC1286/LTC1298

TEST CIRCUITS



APPLICATION INFORMATION

OVERVIEW

The LTC1286 and LTC1298 are micropower, 12-bit, successive approximation sampling A/D converters. The LTC1286 typically draws 250A of supply current when sampling at 12.5kHz while the LTC1298 nominally consumes 350A of supply current when sampling at 11.1 kHz. The extra 100A of supply current on the LTC1298 comes from the reference input which is intentionally tied to the supply. Supply current drops linearly as the sample rate is reduced (see Supply Current vs Sample Rate). The ADCs automatically power down when not performing conversions, drawing only leakage current. They are packaged in 8-pin SO and DIP packages. The LTC1286 operates on a single supply from 4.5V to 9V,

while the LTC1298 operates from a 4.5V to 5.5V supply.

Both the LTC1286 and the LTC1298 contain a 12-bit, switched-capacitor ADC, a sample-and-hold, and a serial port (see Block Diagram). Although they share the same basic design, the LTC1286 and LTC1298 differ in some respects. The LTC1286 has a differential input and has an external reference input pin. It can measure signals floating on a DC common-mode voltage and can operate with reduced spans to 1V. Reducing the spans allows it to achieve 244V resolution. The LTC1298 has a two -channel input multiplexer and can convert either channel with respect to ground or the difference between the two. The reference input is tied to the supply pin.

APPLICATION INFORMATION

SERIAL INTERFACE

The 2-channel LTC1298 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface. The single channel LTC1286 uses a 3-wire interface (see Operating Sequence in Figures 1 and 2).

Data Transfer

The CLK synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems.

The LTC1286 does not require a configuration input word and has no D_{IN} pin. A falling CS initiates data transfer as shown in the LTC1286 operating sequence. After CS falls the second CLK pulse enables D_{OUT} . After one null bit the

A/D conversion result is output on the D_{OUT} line. Bringing CS high resets the LTC1286 for the next data exchange.

The LTC1298 first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: CS, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select (CS) signal. After CS falls the LTC1298 looks for a start bit. After the start bit is received, the 3-bit input word is shifted into the D_{IN} input which configures the LTC1298 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange CS should be brought high. This resets the LTC1298 in preparation for the next data exchange.

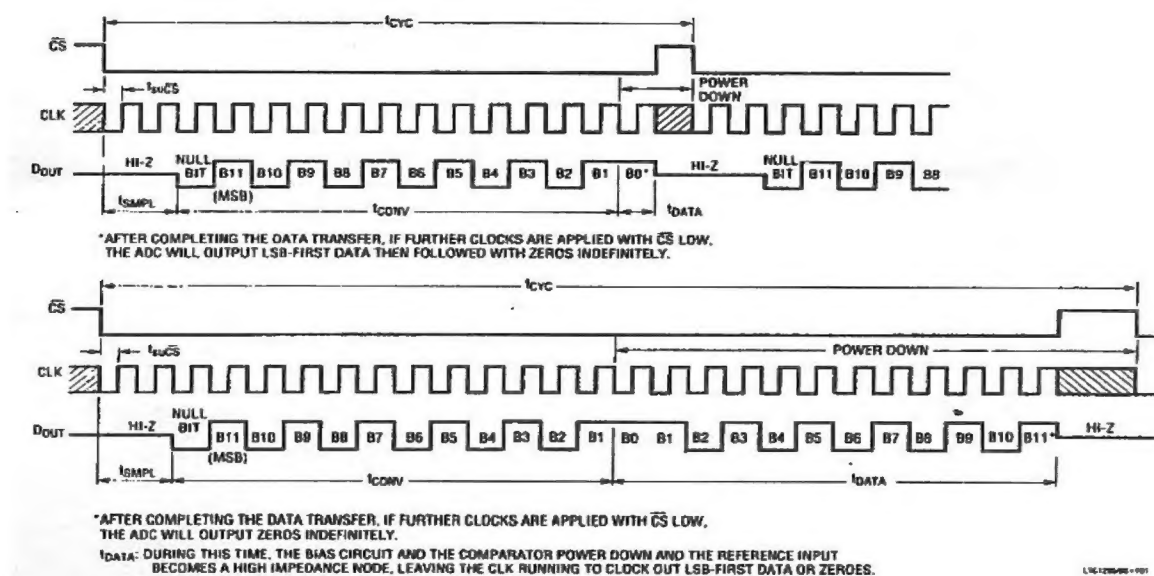
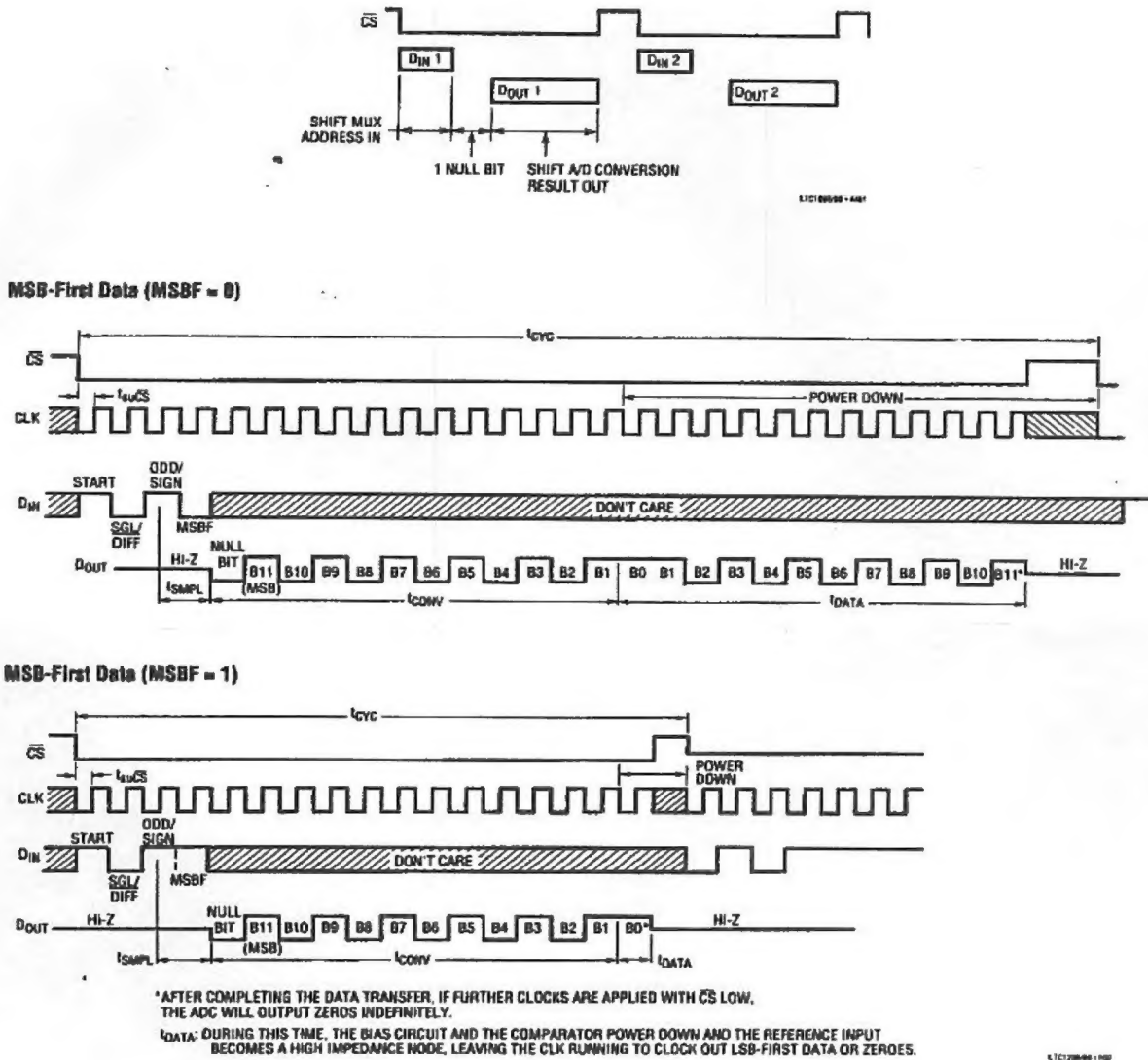


Figure 1. LTC1286 Operating Sequence

LTC1286/LTC1298

APPLICATION INFORMATION

Figure 2. LTC1298 Operating Sequence Example: Differential Inputs (CH⁺, CH⁻)